

Descriptions

RLCS310 is a high performance four-data lane MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The RLCS310 has wide bandwidth and maintains good signal integrity, which makes it ideal is designed for the MIPI specification and allows connection to a CSI or DSI module.

Features

- 2-Differential Channel 1:2/2:1 Mux/De-Mux
- USB 3.1 Super Speed 10Gbps Switch
- MIPI D-PHY Switch
- High Bandwidth: 5.1GHz @ -3dB BW
- Isolation: -40dB @ 2.0 Gbps
- Crosstalk: -31dB @ 2.0 Gbps
- ESD Tolerance: 2kV HBM
- Low bit-to-bit skew, Bidirectional
- Wide VCC Operating Range: 1.5v ~ 5.0v
- Small Packaging, QFN 4 x 4 -24 Lead

Applications

- USB Type-C Ecosystem
- Desktop and Notebook PCs
- Server/Storage Area Networks
- PCI Express Backplanes
- Shared I/O Ports
- FPD LinkII and FPD LinkIII Switching

Order information

Package		Part Number	Top-Side Marking	Quantity per Reel
QFN 4x4 -24L	Tape and Reel	RLCS310QN24/R10	3412	5000PCS

Table-1 Order information

Pin Configuration

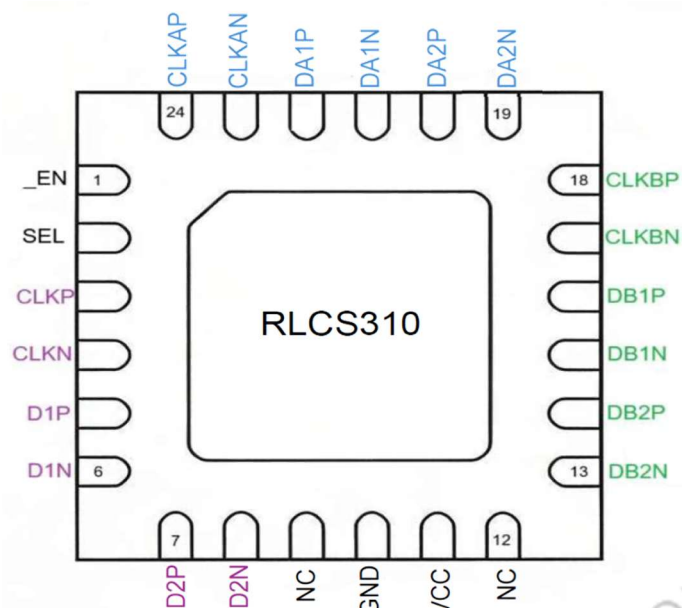


Fig.1 Top-Through View Pin Configuration

Pin Descriptions

Pin#	Pin Name	Signal Type	Description
1	_EN	I	Chip Enable, Active Low
2	SEL	I	Switch logic control
3	CLKP	I/O	Common Side Clock Path Positive
4	CLKN	I/O	Common Side Clock Path Negative
5	D1P	I/O	Common Side Data Path 1 Positive
6	D1N	I/O	Common Side Data Path 1 Negative
7	D2P	I/O	Common Side Data Path 2 Positive
8	D2N	I/O	Common Side Data Path 2 Negative
9,12	NC		Not Connect
10	GND	GND	Ground
11	VCC	Power	Supply Voltage
13	DB2N	I/O	B Side Data Path 2 Negative
14	DB2P	I/O	B Side Data Path 2 Positive
15	DB1N	I/O	B Side Data Path 1 Negative
16	DB1P	I/O	B Side Data Path 1 Positive
17	CLKBN	I/O	B Side Clock Path Negative
18	CLKBP	I/O	B Side Clock Path Positive
19	DA2N	I/O	A Side Data Path 2 Negative
20	DA2P	I/O	A Side Data Path 2 Positive
21	D1N	I/O	Common Side Data Path 1 Negative
22	DA1P	I/O	A Side Data Path 1 Positive
23	CLKAN	I/O	A Side Clock Path Negative
24	CLKAP	I/O	A Side Clock Path Positive

Table-2 Pin Descriptions

Truth Table

_EN	SEL	CLKP	CLKN	D1P	D1N	D2P	D2N
High	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Low	Low	CLKAP	CLKAN	DA1P	DA1N	DA2P	DA2N
Low	High	CLKBP	CLKBN	DB1P	DB1N	DB2P	DB2N

Table-3 Truth Table

Functional Diagram

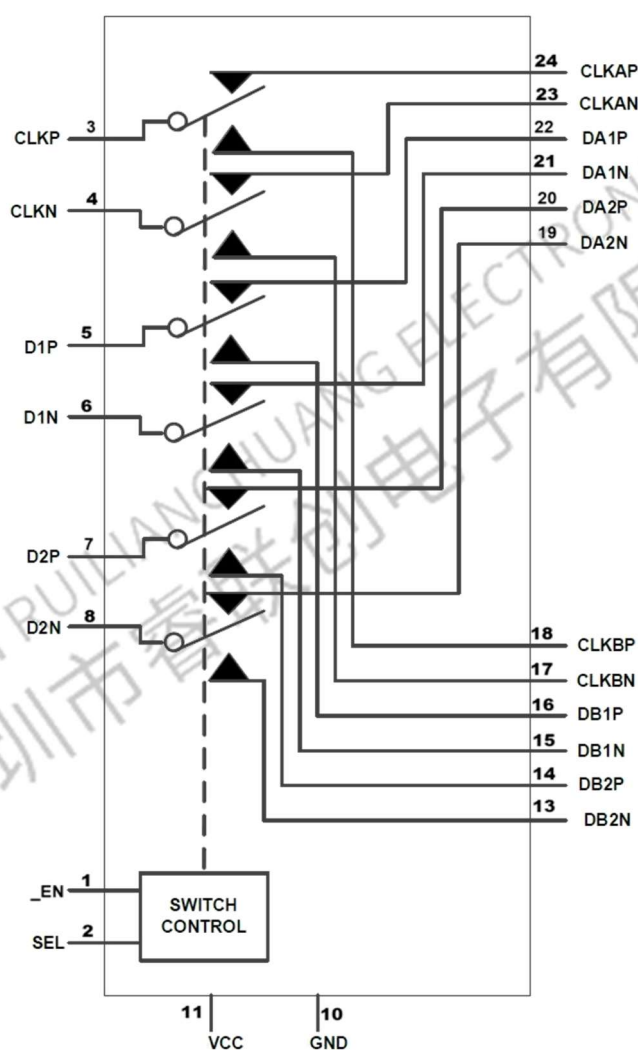


Fig.2 Functional Diagram

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Parameter	Value
Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Supply Voltage to Ground Potential	-0.5V to +5.5V
Supe Speed Data Channel TX / RX	-0.5V to 3.8V
DC Input Voltage	-0.5V to VCC
DC Output Current	50mA
Power Dissipation	300mW

Table-4 Maximum Description**Notes:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics (Ta=25°C, VCC=1.8V, unless otherwise specified)

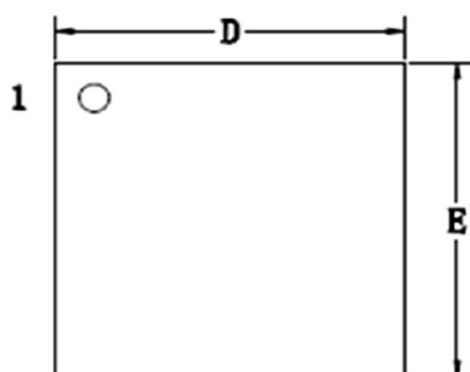
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
VCC Quiescent Current	I _Q	SEL=0 or VCC, _EN=0		28		uA
Power-down Current	I _{PD}	SEL=0 or VCC, _EN=VCC			1	uA
DC CHARACTERISTICS						
Input logic high	V _{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V _{IL}	VCC=1.8~4.5V			0.4	V
_EN Internal pull-up resistor	R _{UP}			2		MΩ
SEL Internal pull-down resistor	R _{DN}			2		MΩ
On-Resistance for Clk/Data	R _{ON_HS}	V _{IS} = 0.2V I _{ON} =8mA		6.7	8	Ω
R _{ON} Flatness for Clk/Data	R _{FLAT_LP}	V _{IS} = 0 to 1.2V I _{ON} =8mA		0.8	1	Ω
R _{ON} Flatness for Clk/Data	R _{FLAT_LP}	V _{IS} = 0 to 0.2V I _{ON} =8mA		0.2	0.3	Ω
R _{ON} Matching Between Channels	R _{MATCH}	V _{IS} = 0 to 1.2V I _{ON} =8mA		0.1		Ω
Switch Off Leakage Current	I _{OFF}	_EN=VCC	-0.5		0.5	uA
AC CHARACTERISTICS						
Enable Time _EN to Output	t _{EN}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		80	150	uS
Disable Time _EN to Output	t _{DIS}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		40	250	nS
Turn-On Time SEL to Output	t _{ON}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t _{OFF}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		130	800	nS
Break-Before-Make Time	t _{BBM}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		250	500	nS
Propagation Delay	t _{PD}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		0.25		nS
Off Isolation	Off	R _L = 50Ω f = 1.2GHz V _{IS} = 0.2V _{PP}		-27		dB
Crosstalk	X _{TALK}	R _L = 50Ω f = 1.2GHz V _{IS} = 0.2V _{PP}		-43		dB
-3dB Bandwidth	BW _{-3dB}	R _L =50Ω C _L =0pF Signal 0dBm	4.5	5.1		GHz
CAPACITANCE						
Switch On Capacitance	C _{ON}	V _{Bias} = 0.2V, f = 1.5GHz		1.5		pF
Switch Off Capacitance	C _{OFF}	V _{Bias} = 0.2V, f = 1.5GHz		1.0		pF

Table-5 Electrical Characteristics

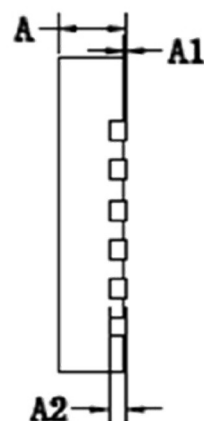
Note:

- (1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.
- (2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.
- (3) Crosstalk is inversely proportional to source impedance

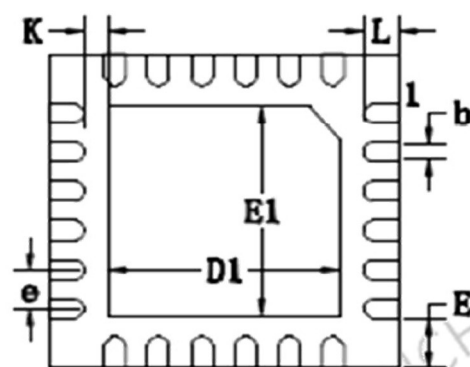
Package Outline Dimensions (QFN 4 x 4 -24L)



顶视图



侧视图



底视图

SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2	0.203 TPY		
b	0.20	0.25	0.30
D	3.95	4.00	4.05
D1	2.55	2.65	2.75
E	3.95	4.00	4.05
E1	2.55	2.65	2.75
E2	0.625 TPY		
e	0.50 BSC		
K	0.275 BSC		
L	0.35	0.40	0.45

Table-6 Package Outline Dimensions

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