

Two-Channel Differential 2:1/1:2 USB 3.1 Super Speed 10Gbps Mux/DeMux

Descriptions

The RLCS3340 is a high-speed bidirectional passive switch for USB Type-C™ applications, supporting USB 3.1 Gen 1/2 data rates. Controlled by the SEL pin, it switches differential channels between Port L0/L1 and Port C0. It's a generic analog switch for high-speed interfaces with a 0 to 2V common mode range and up to 1.8Vpp differential amplitude. Adaptive tracking maintains channel integrity across the common mode range. Its dynamic performance ensures minimal signal attenuation and jitter. Power consumption is <2mW (operational) and <20μW (shutdown via _EN pin). Available in QFN 2x3-18L and QFN 3x3-16L (Pb-/Halogen-free), it's ideal for mobile and space-constrained designs.

Features

- Wide supply range: 1.5V to 5.5V
- 2:1 / 1:2 differential switch/ Multiplexer
- Supports USB 3.1 SuperSpeed (10Gbps)
- High bandwidth: 5.1GHz (@-3dB)
- Isolation: -24dB @ 1.25GHz
- Crosstalk: -34dB @ 1.25GHz
- Low skew, bidirectional
- ESD tolerance: 2kV HBM
- Powered-off protection (VDD = 0V)
- 1.8V-compatible logic inputs

Applications

- USB Type-C™ ecosystem
- Desktop/notebook PCs
- Server/storage networks
- PCIe backplanes
- Shared I/O ports
- FPD-Link II/III switching

Typical Application

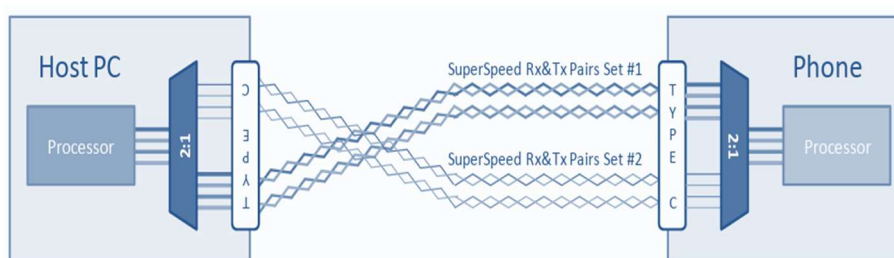


Fig.1 Typical Application

Pin Configuration

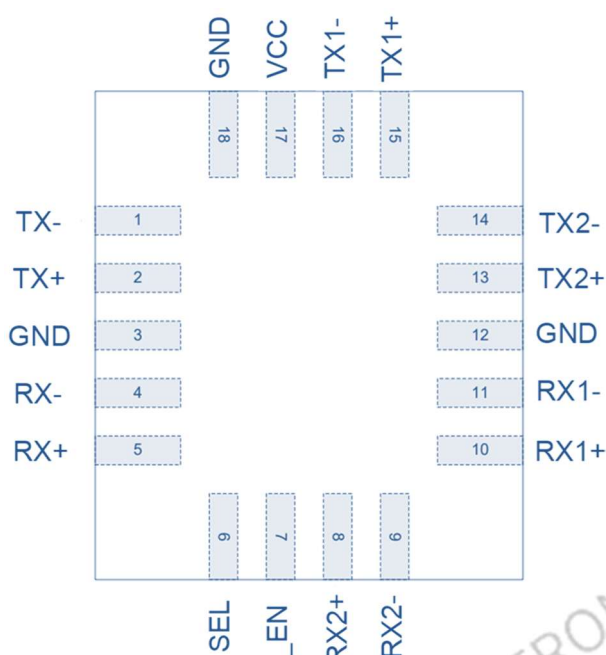


Fig.2 Pin Configuration QFN 2 x 3 -18L

Pin Description (QFN 2 x 3 -18L)

Pin#	Pin Name	Signal Type	Description
1	TX-	I/O	Super Speed TX- Common
2	TX+	I/O	Super Speed TX+ Common
3,12,18	GND	GND	Ground
4	RX-	I/O	Super Speed RX- Common
5	RX+	I/O	Super Speed RX+ Common
6	SEL	I	Switch logic control
7	_EN	I	Chip Enable, Active Low
8	RX2+	I/O	Super Speed RX2+
9	RX2-	I/O	Super Speed RX2-
10	RX1+	I/O	Super Speed RX1+
11	RX1-	I/O	Super Speed RX1-
13	TX2+	I/O	Super Speed TX2+
14	TX2-	I/O	Super Speed TX2-
15	TX1+	I/O	Super Speed TX1+
16	TX1-	I/O	Super Speed TX1-
17	VCC	Power	Supply Voltage

Table-1 Pin Description

Pin Configuration

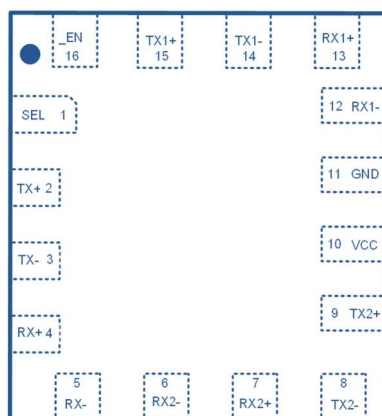


Fig.3 QFN 3 x 3 -16L Pin Configuration

Pin Description (QFN 3 x 3 -16L)

Pin#	Pin Name	Signal Type	Description
1	SEL	I	Switch logic control
2	TX+	I/O	Super Speed TX+ Common
3	TX-	I/O	Super Speed TX- Common
4	RX+	I/O	Super Speed RX+ Common
5	RX-	I/O	Super Speed RX- Common
6	RX2-	I/O	Super Speed RX2-
7	RX2+	I/O	Super Speed RX2+
8	TX2-	I/O	Super Speed TX2-
9	TX2+	I/O	Super Speed TX2+
10	VCC	Power	Supply Voltage
11	GND	GND	Ground
12	RX1-	I/O	Super Speed RX1-
13	RX1+	I/O	Super Speed RX1+
14	TX1-	I/O	Super Speed TX1-
15	TX1+	I/O	Super Speed TX1+
16	_EN	I	Chip Enable, Active Low

Table2 QFN 3x3-16L Pin Description

Truth Table

_EN	SEL	TX+	TX-	RX+	RX-
High	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Low	Low	TX1+	TX1-	RX1+	RX1-
Low	High	TX2+	TX2-	RX2+	RX2-

Table-3 Truth Table

Order Information

Package	Part Number	Quantity per Reel
QFN 2 x 3 -18L	Tape and Reel	RLCS340QN18/R6
QFN 3 x 3 -16L	Tape and Reel	RLCS340QN16/R6

Table-4 Order Information

The diagram illustrates the connection between a Processor and two Type C SS Pairs (1 and 2) via a Type C Connector. The Processor provides control signals: SSRXCOM-, SSRXCOM+, SSTXCOM-, and SSTXCOM+. These signals are connected to a central block containing four multiplexers. The multiplexers are controlled by these signals and output SSRX1-, SSRX2-, SSRX1+, SSRX2+, SSTX1-, SSTX2-, SSTX1+, and SSTX2+. The SSRX signals are connected to the RX pins of the Type C SS Pairs, and the SSTX signals are connected to the TX pins. The SSRX signals are connected directly, while the SSTX signals are connected through capacitors. The central block also has /EN and SEL pins.

Fig.4 Block Diagram

(Above which useful life may be impaired. For user guidelines, not tested.)

Parameter	Value
Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Supply Voltage to Ground Potential	-0.5V to +5.5V
Supe Speed Data Channel TX / RX	-0.5V to 3.8V
DC Input Voltage	-0.5V to VCC
DC Output Current	50mA
Power Dissipation	300mW

Table-5 Maximum Description

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics (Ta=25°C, VCC=1.8V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
VCC Quiescent Current	I _Q	SEL=0 or VCC, _EN=0		28		uA
Power-down Current	I _{PD}	SEL=0 or VCC, _EN=VCC			1	uA
DC CHARACTERISTICS						
Input logic high	V _{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V _{IL}	VCC=1.8~4.5V			0.4	V
_EN Internal pull-up resistor	R _{UP}			2		MΩ
SEL Internal pull-down resistor	R _{DN}			2		MΩ
On-Resistance for TX/RX	R _{ON_HS}	V _{IS} = 0.2V I _{ON} =8mA		6.7	8	Ω
R _{ON} Flatness for TX/RX	R _{FLAT_LP}	V _{IS} = 0 to 1.2V I _{ON} =8mA		0.8	1	Ω
R _{ON} Flatness for TX/RX	R _{FLAT_LP}	V _{IS} = 0 to 0.2V I _{ON} =8mA		0.2	0.3	Ω
R _{ON} Matching Between Channels	R _{MATCH}	V _{IS} = 0 to 1.2V I _{ON} =8mA		0.1		Ω
Switch Off Leakage Current	I _{OFF}	_EN=VCC, Tx, Rx =VCC TX1, TX2, RX1, RX2=0	-0.5		0.5	uA
AC CHARACTERISTICS						
Enable Time _EN to Output	t _{EN}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		80	150	uS
Disable Time _EN to Output	t _{DIS}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		40	250	nS
Turn-On Time SEL to Output	t _{ON}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t _{OFF}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		130	800	nS
Break-Before-Make Time	t _{BBM}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		250	500	nS
Propagation Delay	t _{PD}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		0.25		nS
Off Isolation	Off	R _L = 50Ω f = 1.2GHz V _{IS} = 0.2V _{PP}		-27		dB
Crosstalk	X _{TALK}	R _L = 50Ω f = 1.2GHz V _{IS} = 0.2V _{PP}		-43		dB
-3dB Bandwidth	BW _{-3dB}	R _L =50Ω C _L =0pF Signal 0dBm	4.5	5.1		GHz
CAPACITANCE						
Switch On Capacitance	C _{ON}	V _{Bias} = 0.2V, f = 1.5GHz		1.5		pF
Switch Off Capacitance	C _{OFF}	V _{Bias} = 0.2V, f = 1.5GHz		1.0		pF

Table-6 Electrical Characteristics

Note:

- (1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.
- (2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.
- (3) Crosstalk is inversely proportional to source impedance

Typical Performance Curves (Ta=25°C, VCC=3.0V, CAP=0.1uF, unless otherwise noted)

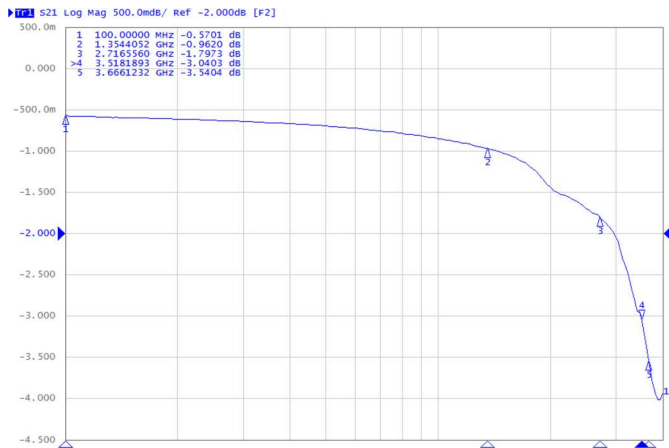


Fig.5 Switch Bandwidth or Insertion Loss

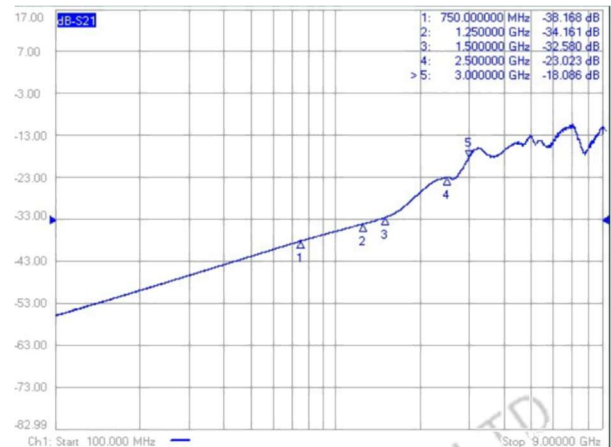


Fig.6 Switch Channel to Channel Cross-Talk

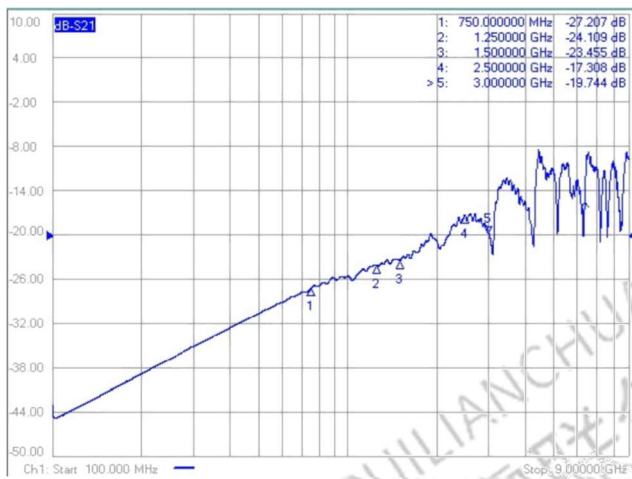
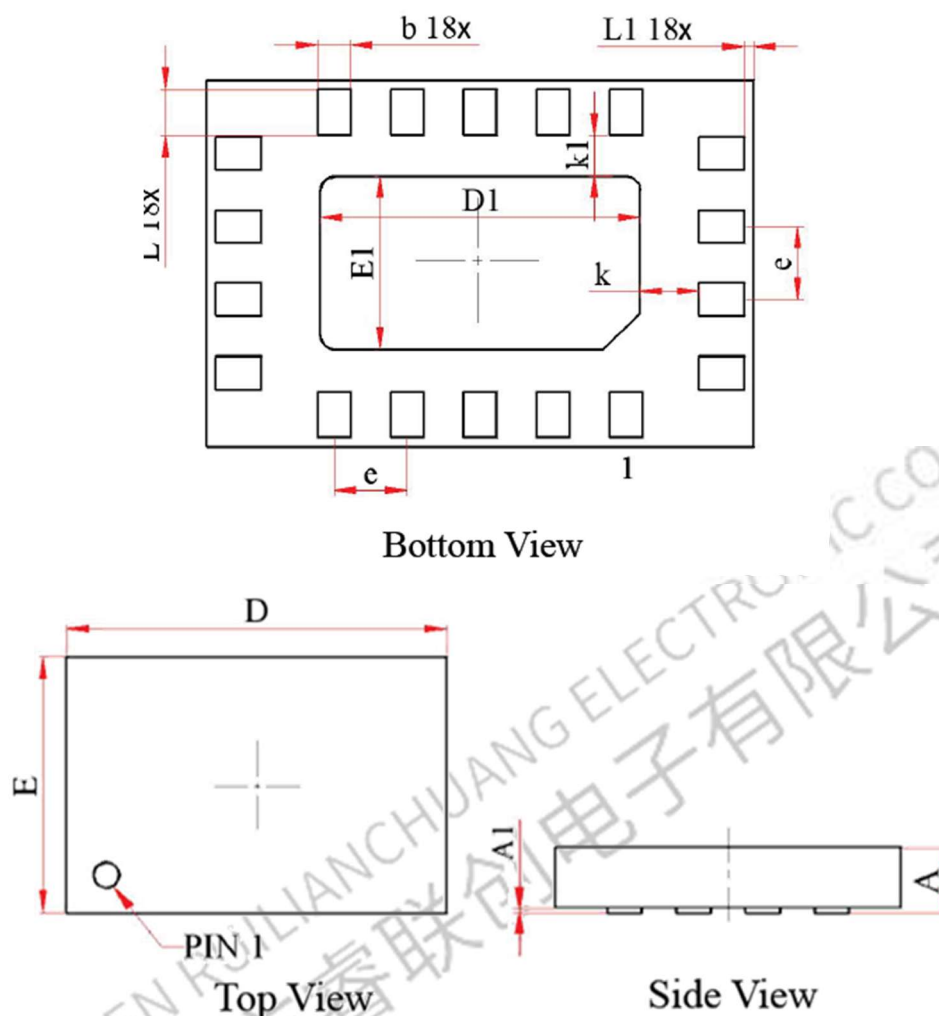


Fig.7 Switch Off Isolation

Package Outline Dimensions

QFN 2 x 3 -18L

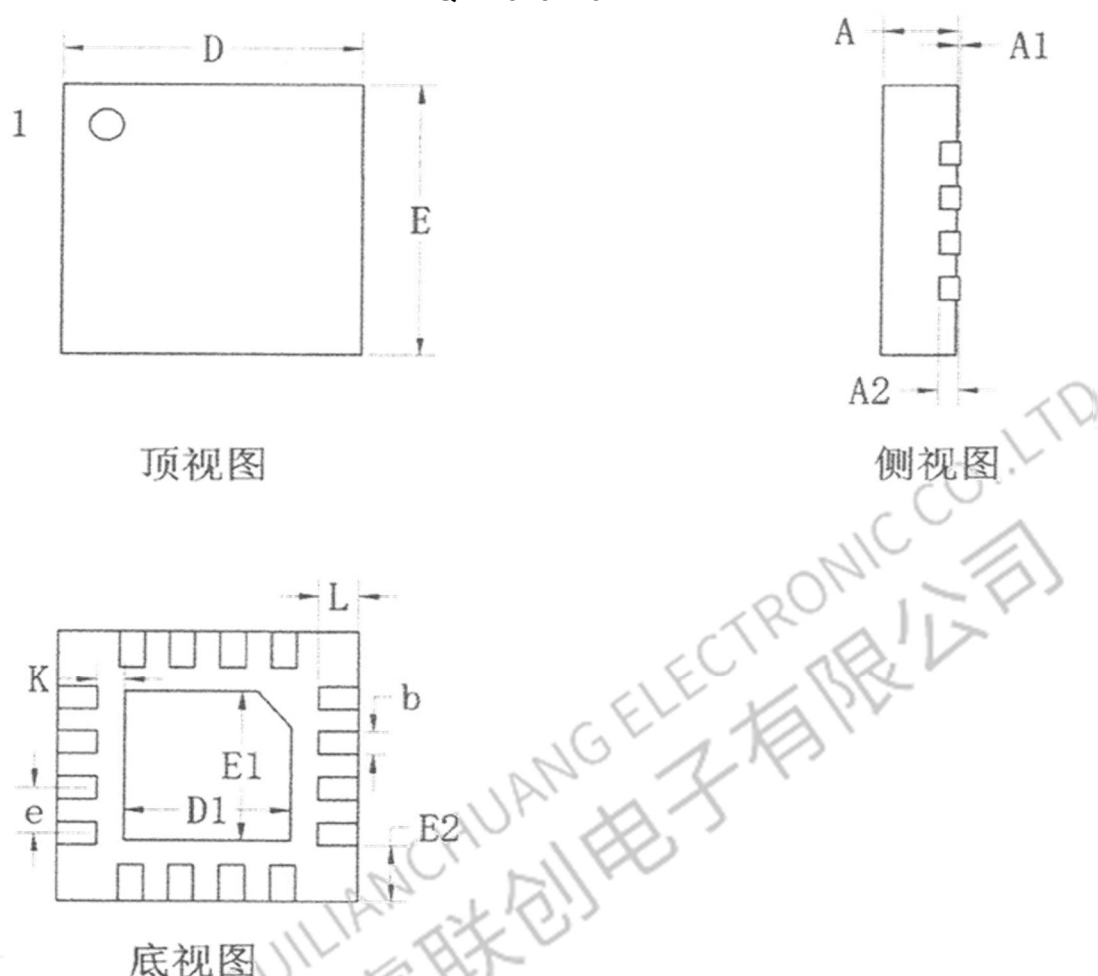


Symbol	Dimension In Millimeters			Dimension In Inches		
	Normal	Min	Max	Normal	Min	Max
A	--	0.340	0.400	--	0.013	0.016
A1	--	0.010	0.050	--	0.000	0.002
D	3.000	2.950	3.050	0.118	0.116	0.120
E	2.000	1.950	2.050	0.079	0.077	0.081
D1	1.750	1.700	1.800	0.069	0.067	0.071
E1	0.950	0.900	1.000	0.037	0.035	0.039
b	0.180	0.150	0.210	0.007	0.006	0.008
L	0.250	0.200	0.300	0.010	0.008	0.012
L1	0.050	0.010	0.090	0.002	0.00	0.004
k	0.325 REF			0.013REF		
k1	0.225 REF			0.009REF		
e	0.400 BSC			0.016 BSC		

Table-6 Package Dimension QFN 2 x 3 -18L

Package outline dimensions

QFN 3x3 -16L



SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0.00		0.05
A2	0.203 TYP		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D1	1.55	1.65	1.75
E	2.95	3.00	3.05
E1	1.55	1.65	1.75
E2	0.625 REF		
e	0.50 BSC		
K	0.275 REF		
L	0.35	0.40	0.45

Table-7 Package Dimension QFN 3 x 3 -16L

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