2:1 MIPI D-PHY (5G bps) 4-Data Lane Switch

Descriptions

RLCS646 is a high performance four-data lane MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The RLCS646 has wide bandwidth and maintains good signal integrity, which makes it ideal is designed for the MIPI specification and allows connection to a CSI or DSI module. 36-Ball Wafer Level Chip Scale Package (WLCSP) 2.4mm x 2.4mm with Pb-free and Halogen-free, makes it ideal for mobile device.

Features

- Wide VCC Supply Range: 1.65V~5.5V
- Low Quiescent Current: 35uA Typical
- Insertion loss: -1dB@1GHz, -2dB@1.5GHz, -3dB@3.5GHz
- Channel-to-Channel Cross-talk: -30dB Typical
- Power-off Truly Isolated and Off-Isolation: -25dB Typical
- 36-Ball WLCSP

Applications

- Laptop
- Multi-Camera and Displays
- 4G/5G Smart Phone
- Mobile and AI Device
- POS camera scan
- Security CIS, Auto-mobile CIS
- Children Watch (e.g.360) with CIS

Order Information

Package		Part Number	Quantity Per Reel
WLCSP 2.4 x2.4 -36 Ball	Tape and Reel	RLCS646WL36/R6	3000PCS

Table-1 Order Information

Pin Configuration

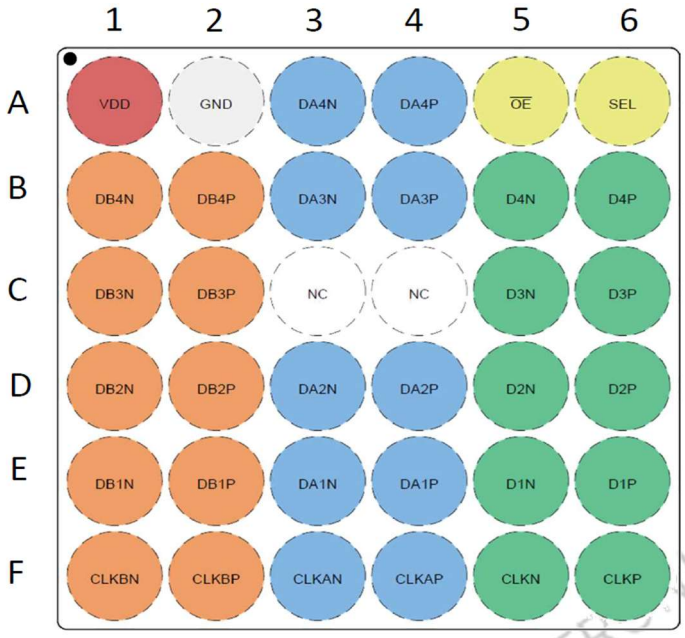


Fig.1 Top-Through View and Top-Side View

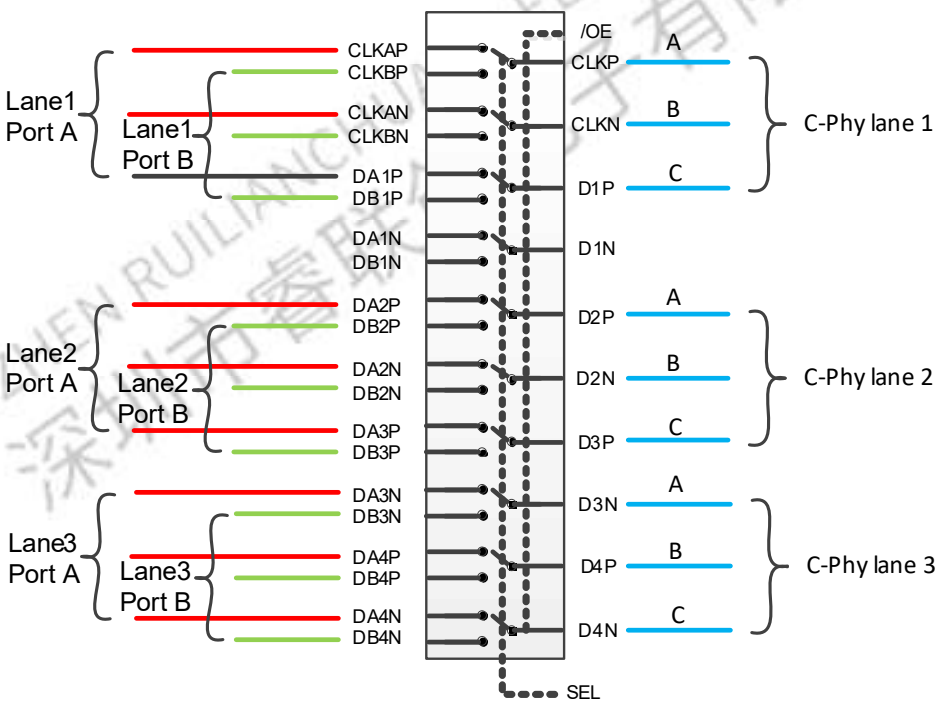


Fig.2 Recommended C-PHY Configuration

Truth Table

SEL	/OE	Function
LOW	LOW	CLKP=CLKAP，CLKN=CLKAN，DN(P/N) =DAN(P/N)
HIGH	LOW	CLKP=CLKBP，CLKN=CLKBN，DN(P/N) =DBN(P/N)
X	HIGH	Clock and Data Ports High Impedance

Table-2 Truth Table

Pin Descriptions

Pin #	Name	Type	Description
A1	VCC	PWR	1.5~5V Positive Supply
A2	GND	GND	Primary Ground Connection. Must be Connected to System Ground
A3	DA4N	I/O	A Side Data Path 4 Negative
A4	DA4P	I/O	A Side Data Path 4 Positive
A5	/OE	I	Chip Enable, Low Active
A6	SEL	I	Channel Selection. When Low, A side selected; When High, B side selected
B1	DB4N	I/O	B Side Data Path 4 Negative
B2	DB4P	I/O	B Side Data Path 4 Positive
B3	DA3N	I/O	A Side Data Path 3 Negative
B4	DA3P	I/O	A Side Data Path 3 Positive
B5	D4N	I/O	Common Side Data Path 4 Negative
B6	D4P	I/O	Common Side Data Path 4 Positive
C1	DB3N	I/O	B Side Data Path 3 Negative
C2	DB3P	I/O	B Side Data Path 3 Positive
C3	NC	O	Not Connected
C4	NC	O	Not Connected
C5	D3N	I/O	Common Side Data Path 3 Negative
C6	D3P	I/O	Common Side Data Path 3 Positive
D1	DB2N	I/O	B Side Data Path 2 Negative
D2	DB2P	I/O	B Side Data Path 2 Positive
D3	DA2N	I/O	A Side Data Path 2 Negative
D4	DA2P	I/O	A Side Data Path 2 Positive
D5	D2N	I/O	Common Side Data Path 2 Negative
D6	D2P	I/O	Common Side Data Path 2 Positive
E1	DB1N	I/O	B Side Data Path 1 Negative
E2	DB1P	I/O	B Side Data Path 1 Positive
E3	DA1N	I/O	A Side Data Path 1 Negative
E4	DA1P	I/O	A Side Data Path 1 Positive
E5	D1N	I/O	Common Side Data Path 1 Negative
E6	D1P	I/O	Common Side Data Path 1 Positive
F1	CLKBN	I/O	B Side Clock Path Negative
F2	CLKBP	I/O	B Side Clock Path Positive
F3	CLKAN	I/O	A Side Clock Path Negative
F4	CLKAP	I/O	A Side Clock Path Positive
F5	CLKN	I/O	Common Side Clock Path Negative
F6	CLKP	I/O	Common Side Clock Path Positive

Table-3 Pin Descriptions

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1)

Parameter	Symbol	Range	Unit
Power Supply Voltage	VCC	-0.5 ~ 6.0	V
Control Pins	_OE, SEL	-0.5 ~ VCC	V
DC Switch I/O Voltage	V_{SW}	-0.3 ~ VCC	V
DC I/O Current	I_{IK}	-50 ~ 50	mA
Storage Temperature Range	T_{STG}	-55 ~ 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001-2012	VCC	±2	kV
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV
ESD MM, JESD22-A115	VCC	±200	V
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV

Table-4 Absolute Maximum Ratings

(1)Stresses beyond those listed in Table-2 Absolute Maximum Ratings may cause permanent damage to the device. They are stress ratings only, which do not imply functional operation of the device at these or any other conditions. Beyond those indicated under Recommended Operating Conditions, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommend Operating Conditions

Parameter	Symbol	Range	Unit
Power Supply Voltage	VCC	1.65 ~ 5.5	V
Control Pins	_OE, SEL	0 ~ VCC	V
Signal Pins	HS Mode	0 ~ 0.3	V
	LP Mode	0 ~ 1.3	V
Operating Temperature	TA	-40 ~ 85	oC

Table-5 Recommend Operating Conditions

(1) If _OE is left undriven, it will be pulled up to VCC by internal resistor; If SEL is left undriven, it will be pulled down to Ground by internal resistor.

Electrical Characteristics (Ta=25℃, VCC=1.8V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
VCC Quiescent Current	IQ	SEL=0 or VCC, _OE=0		30		uA
Power-down Current	IPD	SEL=0 or VCC, _OE=VCC			1	uA
DC CHARACTERISTICS						
Input logic high	VIH	VCC=1.8~4.5V	1.6			V
Input logic low	VIL	VCC=1.8~4.5V			0.4	V
_OE Internal pull-up resistor	RUP			2		MΩ
SEL Internal pull-down resistor	RDN			2		MΩ
On-Resistance for LP MIPI	RON_LP	VIS=1.2V, ION=8mA		4.8	10	Ω
On-Resistance for HS MIPI	RON_HS	VIS=0.2V, ION=8mA		4.3	9	Ω
RON Flatness for LP MIPI	RFLAT_LP	VIS=0 to 1.2V ION=8mA		0.9		Ω
RON Flatness for HS MIPI	RFLAT_LP	VIS=0 to 0.2V ION=8mA		0.2		Ω
RON Matching Between Channels	RMATCH	VIS=0 to 1.2V ION=8mA		0.1		Ω
Switch Off Leakage Current	IOFF	_OE=VCC Dn, Dp =VCC DAn, DBn, DAp, DBp=0 CLKn, CLKp=0 CLKAn,CLKBn, CLKAp, CLKBp=VCC	-0.5		0.5	uA
AC CHARACTERISTICS						
Enable Time _OE to Output	tEN	RL=50Ω CL=0pF VIS=0.6V		80	150	uS
Disable Time _OE to Output	tDIS	RL=50Ω CL=0pF VIS=0.6V		40	250	nS
Turn-On Time SEL to Output	tON	RL=50Ω CL=0pF VIS=0.6V		400	1200	nS
Turn-Off Time SEL to Output	tOFF	RL=50Ω CL=0pF VIS=0.6V		130	800	nS
Break-Before-Make Time	tBBM	RL=50Ω CL=0pF VIS=0.6V		250	500	nS
Propagation Delay	tPD	RL=50Ω CL=0pF VIS=0.6V		0.25		nS
HS Mode Skew of Opposite Transitions of the Same	tSK(P)	RL=50Ω CL=0pF VIS=0.3V		6		pS

Output						
HS Mode Skew of Channel-to-Channel Single-Ended Skew	tSK(O)	RL=50Ω CL=0pF VIS= 0.3V		6		pS
Off Isolation	Off	RL= 50Ω f=1.2GHz VIS=0.2VPP		-25		dB
Crosstalk (Channel-to-Channel)	XTALK	RL= 50Ω f= 1.2GHz VIS= 0.2VPP		-30		dB
-3dB Bandwidth (Insertion Loss)	BW-3dB	RL=50Ω CL=0pF Signal 0dBm		3.5		GHz
CAPACITANCE						
Switch On Capacitance	CON	VBias=0.2V, f= 1250MHz		1.5		pF
Switch Off Capacitance	COFF	VBias=0.2V, f= 1250MHz		1.0		pF

Table-6 Electrical Characteristics

Note:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) RON matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

Functional Diagram

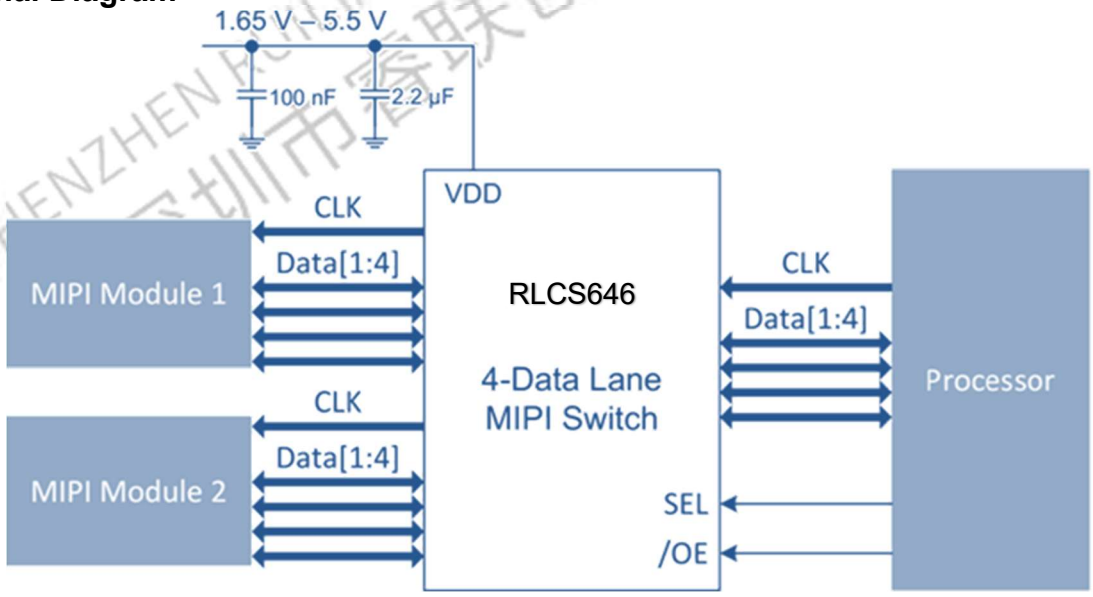


Fig.3 Functional Diagram

Typical Performance Curves (Ta=25℃, VCC=3.0V, CAP=0.1uF, unless otherwise noted)

Fig.4 Switch Bandwidth or Insertion Loss

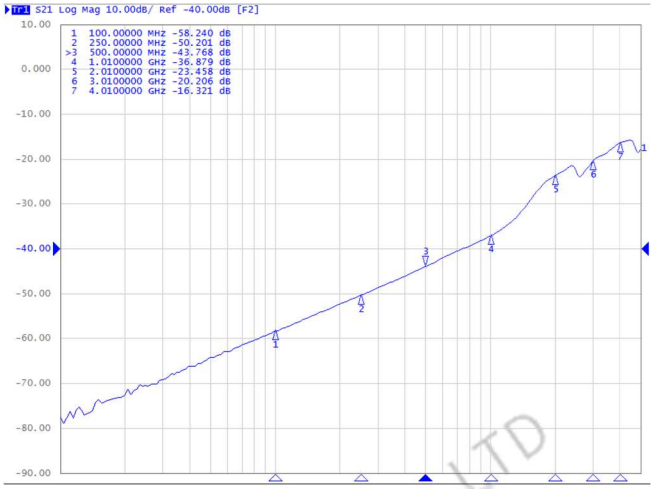


Fig.5 Switch Channel to Channel Cross-Talk

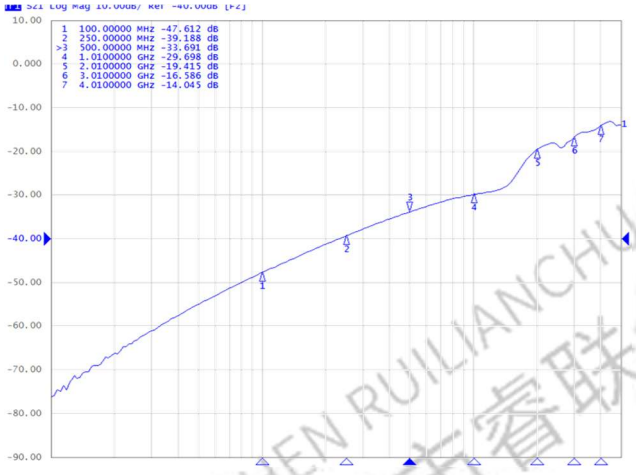


Fig.6 Switch Off Isolation

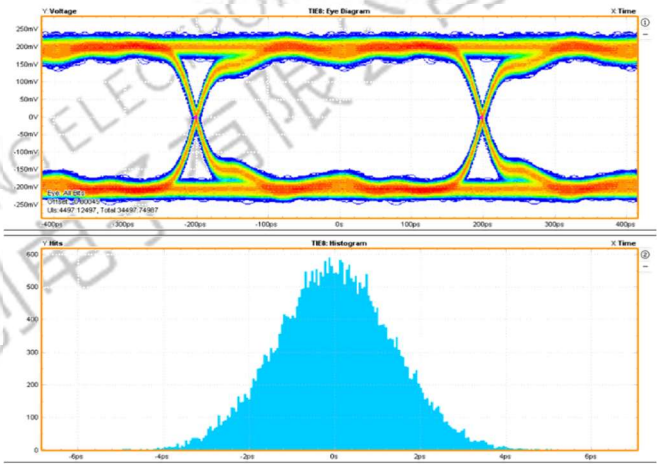
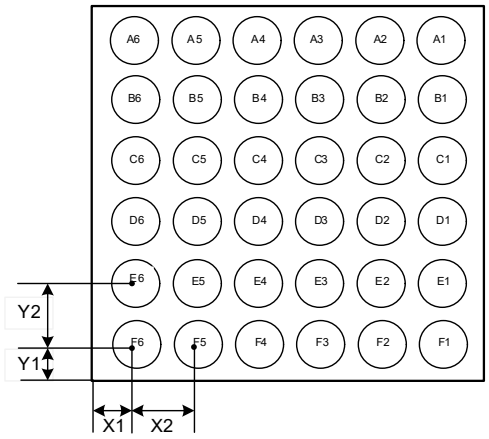


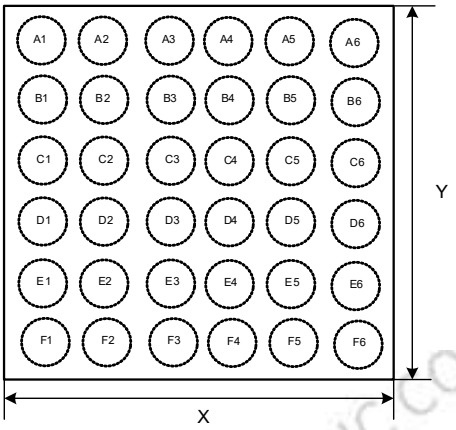
Fig.7 Eye Diagram

Package Outline Dimensions

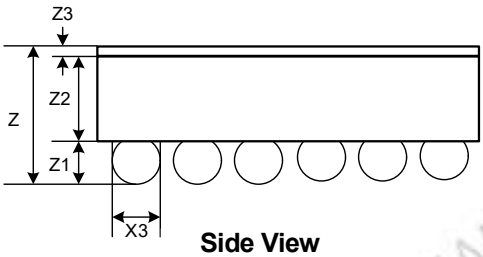
WLCSP-36B



Bottom-Up View



Top-Through View



Side View

Fig.8 Package Outline Dimensions

Symbol	Dimensions In Millimeter		
	Min.	Typ.	Max.
X	2.37	2.40	2.43
Y	2.37	2.40	2.43
X1		0.16	
X2		0.40	
X3	0.175	0.205	0.235
Y1		0.16	
Y2		0.40	
Z	0.550	0.600	0.650
Z1	0.145	0.170	0.195
Z2	0.340	0.365	0.390
Z3	0.395	0.040	0.045

Table-7 Package Outline Dimensions

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